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# 2306

# B. E./B. Tech. 6th Semester (AEIE) Examination – May, 2014

## DIGITAL SYSTEM DESIGN

### Paper : EE-310-E

*Time : Three Hours ]*      *[ Maximum Marks : 100*

*Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.*

*Note :* Attempt any *five* questions. All questions carry equal marks.

**1.** (a) Discuss in detail about different classes of VHDL objects with suitable examples.      14

     (b) Explain the difference between :      6

       (i) Signal and Variable

**2.** (a) Write entity declaration for the following : 3 × 4

    (i) Half Adder,

    (ii) S-R Flip Flop,

    (iii) 2 : 4 decoder,

    (iv) 4 bit comparator.

  (b) Discuss in brief about different delay models in VHDL. 8

**3.** (a) Write VHDL code for 4 : 1 multiplexer using : 10

    (i) Case Statement,

    (ii) IF Then Else Statement.

  (b) Design a 16 : 1 multiplexer using 8 : 1 multiplexer. Write VHDL code for same. 10

**4.** Explain the following : 7, 7, 6

  (i) Subprogram overloading,

  (ii) Libraries and packages,

5. Design a full adder using two half adders. Draw the circuit diagram and VHDL code for same. Also write VHDL code for design of full adder using behaviour style of modelling. 20

6. Write VHDL code for following : 6, 7, 7

   (i) 4 bit serial in Parallel out Register,

   (ii) MOD-10 ripple Counter using J-K flip flops,

   (iii) 3 bit binary to gray code converter.

7. (a) What are generics ? Draw the logic diagram and write VHDL code for n input AND gate using generics. 14

   (b) What is configuration declaration ? Explain with example. 6

8. (a) Design a 4 bit ALU in VHDL. 10

   (b) Implement $F(A, B, C) = \sum(2, 4, 6, 7)$ using PLA.

   10